Remarks

Allowance of all pending claims is respectfully requested. Claims 1-7, 10-14 & 30-35 remain pending.

By this paper, claim 1 is amended to specify that the first solder bumps comprise first reflowed solder bumps and the second solder bumps comprise second reflowed solder bumps. Additionally, claim 1 is amended to specify that the second reflowed solder bumps comprise alignment solder bumps which aligned the first reflowed solder bumps between the first substrate and the second substrate before the first reflowed solder bumps were reflowed. Claim 30 is amended to specify that the second solder bumps comprise alignment solder bumps which when melted align the first substrate to a second substrate before melting of the first solder bumps. Thus, in the amendments to both claims 1 & 30, applicants further specify that both the first solder bumps and the second solder bumps are melted (i.e., reflowed), or are to be melted (i.e., are to be reflowed). Support for the amendments to these independent claims can be found throughout the application as followed. For example, reference specification pages 10 & 13-14, as well as FIGs. 6A-6C. No new matter is added to the application by any amendment presented.

In the Office Action, claims 1, 30, 34 and 35 were rejected under 35 U.S.C. 102(e) as being anticipated by Downes (U.S. Patent No. 6,222,277), and claims 1-3, 5-7, 10, 11 and 30-35 were rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. (U.S. Patent No. 6,225,700). In addition, claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. in view of Behun et al. (U.S. Patent No. 5,060,844), and claims 12-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. in view of Bertin et al. (U.S. Patent No. 5,977,640). These rejections are respectfully, but most strenuously, traversed to any extent deemed applicable to the claims presented herewith and reconsideration thereof is requested.

Current solder bump array deposition technologies require an expensive and time consuming mask alignment process. This alignment process becomes increasingly difficult and costly as the solder bump size and pitches decrease. To realize the full advantages of multi-chip stack technology, very high solder bump interconnect density is needed. Unfortunately, the multi-chip stack structure may suffer the expensive and inherent technology limitations

associated with current solder bump array technologies. Applicants claimed invention is designed to address these inherent limitations by providing a self-aligning interconnect structure.

As recited in claim 1, for example, applicants' invention comprises a structure which has a first substrate and a second substrate, and first reflowed solder bumps and second reflowed solder bumps offset therebetween. The first reflowed solder bumps and the second reflowed solder bumps are separate solder bumps disposed between the first substrate and the second substrate, and the second reflowed solder bumps have at least a portion that melts at a lower temperature then the first reflowed solder bumps. Further, functionality is recited to the effect that the second reflowed solder bumps comprise alignment solder bumps which aligned the first reflowed solder bumps between the first substrate and the second substrate before the first reflowed solder bumps were melted. A similar characterization is also present in independent claim 30, wherein applicants recite that the second solder bumps comprise alignment solder bumps which when melted align the first substrate to a second substrate before melting of the first solder bumps. Applicants recited structure of independent claims 1 & 30 is clearly distinct from the teachings and suggestions of both Downes and Ito et al.

It is well settled that there is no anticipation of a claim unless a single prior art reference discloses: (1) all of the same elements of a claimed invention; (2) found in the same situation as the claimed invention; (3) united in the same way as the claimed invention; and (4) in order to perform the identical function of the claimed invention. In this instance, both Downes and Ito et al. fail to disclose various elements of applicants' invention as recited in amended independent claims 1 & 30, and as a result, do not anticipate (or even render obvious) applicants' invention.

Downes discloses a non-collapsing stand-off for semiconductor devices. The structure includes a plurality of balls formed of a first solder alloy disposed on the bottom surface of the semiconductor substrate and projecting downwardly therefrom. Each of the plurality of balls is sized to support the weight of the semiconductor substrate. The structure also includes a plurality of solder joints formed of a second solder alloy connecting the plurality of balls to the corresponding plurality of wettable pads on the printed circuit board. The first solder alloy has a liquidus temperature greater than the second solder alloy liquidus temperature, and the second solder alloy has a liquidus temperature suitable for use with the material comprising the printed

circuit board and the semiconductor substrate. The material comprising the printed circuit board and the semiconductor substrate are thermally degradable at a temperature greater than the liquidus temperature of the second solder alloy and less than the liquidus temperature of the first solder alloy. (See Abstract of Downes.)

Initially, applicants note that Downes does not discuss the problem addressed by the present invention (i.e., how to achieve better alignment of fine pitched solder bumps). Rather, Downes is addressing how to establish a minimum fixed spacing between a semiconductor substrate and a printed circuit board using an interconnect structure. In Downes, this is achieved by providing a first plurality of balls 40 of a first solder alloy having a liquidus temperature greater than the liquidus temperature of a second plurality of solder balls 41. As explained in Downes, the temperature to which the assembly is heated always remains below the liquidus temperature of the solder alloy comprising the plurality of balls 40. (See Col. 9, lines 35-59.)

In contrast, applicants' amended claim 1 characterizes the first solder bumps and the second solder bumps as first reflowed solder bumps and second reflowed solder bumps, respectively. In applicants' invention, both types of solder bumps are reflowed. Downes thus expressly teaches away from applicants' invention by indicating that the plurality of solder balls 40 are not to be melted. In fact, if one were to propose a modification in Downes to melt solder balls 40, then the intended purpose of Downes would be negated.

Still further, applicants recite that the second reflowed solder bumps comprise alignment solder bumps which align the first reflowed solder bumps between the first substrate and the second substrate before the first reflowed solder bumps are melted (claim 1), or alternatively, comprise alignment solder bumps, which when melted align the first substrate to a second substrate before melting of the first solder bumps. Applicants respectfully submit that Downes does not teach or suggest this functionality. As noted above, the first plurality of solder balls 40 in Downes are not to be reflowed (contrary to applicants' recited structures). In applicants' invention, the reflowing of the second solder bumps provides a further level of alignment between the first and second substrates prior to reflowing of the first solder bumps.

In this regard, applicants respectfully traverse the conclusion at page 3 of the Office Action (and subsequent pages) that applicants' Best Mode discussion, which discloses the

recognition that the reflow process inherently causes alignment, can be employed to reject their claimed invention. Applicants respectfully submit that this justification does not identify an adequate teaching or suggestion in Downes which would indicate their claimed invention as being anticipated thereby. Applicants respectfully submit that the only suggestion for reflowing the second solder bumps to provide another level of alignment between a first and second substrate is disclosed in applicants' own specification, which as well known, cannot be used as a reference against their claimed invention. It is applicants who have discovered that reflowing of second solder bumps as recited in the independent claims provides a further level of alignment between the first and second substrate which further facilitates precise alignment of the first solder bumps, before the first solder bumps are melted.

For the above reasons, applicants respectfully submit that amended independent claims 1 & 30 patentably distinguish over the teachings of Downes. Reconsideration and withdrawal of the rejection based thereon is therefore requested.

Ito et al. describe a package for a semiconductor element having depressions containing solder terminals. A plurality of terminals 4 are employed to electrically connect a semiconductor device to an electrical circuit board. Terminals 4 comprise solder, which when reflowed electrically connects the semiconductor device to the printed circuit board. Additionally, a plurality of metal balls 10 are provided to form a fixed gap between the lower surface of the insulating substrate 1 and the upper surface of the external electrical circuit board B. The metal balls 10 are formed of copper, which also has good heat conductive properties.

With respect to Ito et al., applicants again note that metal balls 10 in Ito et al. are designed not to melt or reflow, but rather are designed to function as a spacer to define a fixed gap between the lower surface of insulating substrate 1 and the upper surface of the external electrical circuit board B. Thus, applicants respectfully submit that independent claims 1 & 30 patentably distinguish over Ito et al. for the reasons noted above with respect to Downes. Ito et al. does not disclose: (1) first reflowed solder bumps and second reflowed solder bumps; nor (2) that the second reflowed solder bumps comprise alignment solder bumps which align the first reflowed solder bumps between the first substrate and the second substrate before the first reflowed solder bumps are melted.

Further, applicants' independent claims expressly recite first reflowed solder bumps and second reflowed solder bumps. The copper balls 10 of Ito et al. are simply spacing metallurgy to provide a minimum fixed space between the semiconductor device and printed circuit board. One skilled in the art would not read the teachings thereof as somehow suggesting that copper balls 10 are a "solder bump". The phrase "solder bump" refers to a particular metallurgy, which is distinct from copper pads or copper lines on the adjoining structure. Thermal cycling is employed to melt a solder bump and electrically interconnect two structures. Copper pads or balls do not melt during this thermal cycling. In fact, it would be impossible in Ito et al. to melt the copper balls, since the laminate on which the balls are disposed would be destroyed as well as any copper lines which may be present. Thus, applicants respectfully traverse the characterization of copper balls 10 as a "solder bump" functionally equivalent to applicants' recited structure. Applicants application is directed to a structure having "first reflowed solder bumps" and "second reflowed solder bumps". Because of this, applicants respectfully submit that one of ordinary skill in the art would not have read the teachings of Ito et al. as disclosing their recited solder bumps. Again, the "bump" 10 in Ito et al. is copper, which is a different metallurgy and does not melt or reflow during the fabrication process.

In addition, a careful reading of Ito et al. fails to uncover any teaching or suggestion of two different types of solder bumps, with one type of solder bump having a melting temperature that is different from the other type of solder bump. Metal balls 10 comprise copper in Ito et al. and simply do not equate to applicants recited "solder bumps".

Further, applicants recite that the second reflowed solder bumps (or second solder bumps) comprise alignment solder bumps which align the first reflowed solder bumps between the first substrate and the second substrate before the first reflowed solder bumps are melted. This functionality is believed clearly distinct from any teaching of suggestion in Ito et al. There is no alignment in Ito et al. of first solder bumps using second solder bumps before the first solder bumps are reflowed, nor is there any teaching or suggestion in Ito et al. that this alignment using the second solder bumps results from reflowing of the second solder bumps.

In view of the differences noted above, applicants respectfully submit that their invention as recited in independent claims 1 & 30 would not have been anticipated (or even rendered

obvious) by the structures of Ito et al. Therefore, reconsideration and withdrawal of the anticipation rejection based thereon is respectfully requested.

The dependent claims are believed patentable for the same reasons as the independent from which they directly or ultimately depend, as well as for their own additional characterizations. In this regard, applicants respectfully submit that neither Behun et al., nor Bertin et al. teach or suggest the above-noted deficiencies of Downes and Ito et al. when applied against applicants' amended independent claims. Applicants respectfully request reconsideration and withdrawal of the obviousness rejections contained in the Office Action for the reasons stated above in connection with independent claims 1 & 30.

The application is believed to be in condition for allowance and such action is respectfully requested.

Applicants' undersigned attorney is available should the Examiner wish to discuss this application further.

Respectfully submitted,

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